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N-channel operation of pentacene thin-film transistors
with ultrathin polymer gate buffer layer

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(Abstract)

N-channel operation of pentacene thin-film transistors with ultrathin poly(methyl methacrylate) (PMMA) gate buffer layer and gold source-drain electrode was observed. We prepared pentacene thin-film transistors with an 8-nm-thick PMMA buffer layer on SiO₂ gate insulators and obtained electron and hole field-effect mobilities of 5.3×10^{-2} cm²/(Vs) and 0.21 cm²/(Vs), respectively, in a vacuum of 0.1 Pa. In spite of using gold electrodes with a high work function, the electron mobility was considerably improved in comparison with previous studies, because the ultrathin PMMA film could decrease electron traps on SiO₂ surfaces, and enhance the electron accumulation by applied gate voltages.

(Keywords) gate buffer layer, electron trap, ambipolar transport, organic thin-film transistor, pentacene

1. Introduction

Control of the conduction type in organic thin-film transistors (OTFTs) is one of the most important issues to be solved for realizing their practical application such as organic complementary circuits (CMOS) and light emitting devices [1]. It is well known that a large part of π -conjugated molecules are so-called *p*-type semiconductors in air, although newly-synthesized molecules with a small bandgap [2] or high electron affinity [3] can be employed as *n*-type even in air. However, the carrier transport in organic devices is greatly influenced by several outer factors. For example, the type of majority carrier depends on the degree of vacuum and the kind of gas atmosphere [4]. Moreover, the electron injection from metal electrodes with low work functions (e.g., aluminum and calcium) into organic semiconductor layers causes *n*-channel conduction even in transistors based on *p*-type semiconductors [5,6]. Recently, many single-component *p*-channel OTFTs were driven in *n*-channel operation by utilizing polymer gate dielectrics [7-9] and inserting polymer layers into semiconductor/oxide-insulator interfaces [10-13].

Even pentacene thin-film transistors, which are well known for its large hole field-effect mobility ($\sim 1 \text{ cm}^2/(\text{Vs})$), were reported to show *n*-channel operation with various methods described above [5-8,10,13]. However, the electron field-effect

mobility of pentacene transistors reported in previous works was still much smaller than the hole mobility. It has been theoretically suggested that organic semiconductors, in general, can be good transporters for both electron and hole [14]. The achievement of high mobility for both electron and hole has been strongly required in terms of both industrial and academic viewpoints, e.g. for realizing high-performance, low-cost CMOS with OTFTs, and for understanding the carrier injection/transport mechanism in organic semiconducting devices.

Here, we demonstrated *n*-channel operation of pentacene TFTs with gold (Au) source-drain electrode, by depositing an 8-nm-thick poly(methyl methacrylate) (PMMA) film onto a SiO₂ gate dielectric. In our previous works, the increase of the electron mobility for *n*-channel OTFTs based on *N,N'*-ditridecyl-3,4,9,10-perylenetetracarboxylic diimide (PTCDI-C13) [15] and 1,4,5,8-naphthalene tetracarboxylic dianhydride (NTCDA) [16] were observed by utilizing this ultrathin PMMA gate buffer layer, although electron injection barrier between a work function of Au electrode (5.1 eV) and LUMO (lowest unoccupied molecular orbital) of *n*-type semiconductors (PTCDI-C13 (4.0 eV) [3] and NTCDA (3.6 eV) [17]) was expected to be large. Similarly to the study on these *n*-channel transistors, a high electron field-effect mobility ($5.3 \times 10^{-2} \text{ cm}^2/(\text{Vs})$) for pentacene TFTs was also

obtained in this work despite a large electron injection barrier between Au electrode and LUMO of pentacene (3.2 eV) (Fig. 1(a)) [5]. The influence of the PMMA spacer on *n*-channel operation of pentacene transistors was considered.

2. Experimental Procedure

Pentacene and PMMA were purchased from Aldrich. A PMMA layer was deposited by spin-coating onto a thermally-grown SiO₂ on heavily doped *n*-type silicon wafer. The nominal thickness of the SiO₂ layer was 100 nm. The details of preparation of the PMMA film were described elsewhere [15,16,18]. The X-ray reflectivity (XR) measurement for the ultrathin PMMA film was performed with a commercial measurement system (ATX-G, Rigaku) using Cu K_α radiation. The XR profiles were analyzed with a Rigaku GXRR data-fitting software based on the theory of Parratt [19]. Ellipsometric measurements were performed for PMMA films thicker than 100 nm, using a DHA-FX (Mizojiri Optical Ltd.).

Pentacene was purified by sublimation twice and thermally evaporated onto SiO₂ coated with PMMA under a pressure of 1.0×10^{-4} Pa. The thickness of pentacene films and the substrate temperature were set to be 50 nm and 338 K, respectively. Successively, the pentacene film specimens were transferred into another metal

deposition chamber with a short air exposure for ten minutes, and 25-nm-thick Au source-drain electrode with the channel length (L) of 50 μm and width (W) of 1 mm was deposited onto the pentacene films. Thus, top-contact transistors were fabricated as shown in Fig. 1(b).

The prepared TFTs were taken out from the evaporation chamber and put into a vacuum probe system (ST-500, JANIS) within ten minutes after this temporary air exposure of specimens. Then, transistor characteristics were measured in a vacuum (0.1 Pa), with a Keithley 4200-SCS semiconductor parameter analyzer. The field-effect mobility for electron (μ_e) and hole (μ_h) and threshold voltage (V_T) were calculated from transfer characteristics (drain-source saturation current ($I_{D,\text{sat}}$) vs. gate voltage (V_G)) according to the following equation;

$$I_{D,\text{sat}} = WC_i\mu_{e(h)}(V_G - V_T)^2/(2L), \quad (1)$$

where C_i is the gate capacitance. Here C_i was determined by an LCR meter (HP4263A, Agilent) at a frequency of 100 Hz, by using a stacking structure of PMMA, SiO_2 and a heavily-doped Si substrate, on which upper Au electrodes were deposited by vacuum evaporation. The measured C_i values for the PMMA/ SiO_2 layers employed in this work were smaller than the measured value for the SiO_2 film (30.7 nF/cm²), confirming that unintended increase of C_i due to the existence of PMMA did not occur.

The surface morphology of pentacene films was observed with an atomic force microscope (AFM) (JSPM-5200, JEOL) and the crystal structure was examined using an X-ray diffractometer (XRD) (MXP³, BrukerAXS) with Cu K α radiation.

3. Experimental results

3.1 *Characterization of the ultrathin PMMA layer and pentacene thin films*

A result of XR measurement for the stacking structure of PMMA, SiO₂ layers and a Si substrate was shown in Fig. 2. An interference fringe (Kiessig fringe) owing to the ultrathin PMMA layer was observed clearly. From the best-fitted curve for the experimental result, the thickness of 8.0 nm, the density of 1.19 g/cm³, and the surface roughness of 0.33 nm were estimated for the PMMA film, respectively. And the thickness of the SiO₂ layer was calculated to be 106.3 nm at the same time. This result suggests that PMMA was deposited uniformly over the whole surface of SiO₂, since the surface roughness was very small and the density was the same as that of bulk PMMA (1.19 g/cm³). The capacitance of the double layer of this 8-nm-thick PMMA and SiO₂ was measured to be 29.3 nF/cm².

Figure 3 shows AFM images and XRD profile of pentacene thin films. For comparison, the surface morphology of pentacene films prepared on a bare SiO₂ under

the same evaporation condition was also shown there. In our experiment, the grain size of pentacene films on PMMA was on average smaller than that of films on SiO₂. Recently, the surface morphology of pentacene on various polymer dielectrics such as poly(4-vinylphenol) (PVP) [8], poly(vinyl alcohol) (PVA) [8, 20], PMMA [20] and so on, has been discussed in terms of the surface energy, and it was reported that PMMA layer promotes grain growth of pentacene [20]. However, we could not observe such an effect in this work. The pentacene film on PMMA showed sharp X-ray diffraction peaks of (00*l*) (*l*=1-5) reflection of a thin-film phase, accompanied with smaller peaks of (00*m*) (*m*=1-4) reflection of a bulk phase [21]. The larger ratio of the thin-film phase in pentacene films can lead to the higher field-effect mobility because it is thought that π -overlap in the plane of the substrate in the thin-film phase is greater than in the bulk phase [21]. Therefore, good carrier transport between source and drain electrodes was expected in this pentacene film on the PMMA spacer.

3.2 *Characterization of the pentacene TFT with the ultrathin PMMA layer*

Figure 4 presents output characteristics (drain-source current (I_D) vs. drain-source voltage (V_D)) of pentacene TFTs with the 8-nm-thick PMMA layer. The device displayed a typical *p*-channel operation for negative V_D and V_G as shown in Fig.

4(a). In the configuration of n -channel operation (positive V_D and V_G), the drastic increase of current with increasing V_D was observed at lower V_G . At $V_G > 70$ V, the saturation of the drain current for increasing V_D occurred as shown in Fig. 4(b), proving an ambipolar operation of the TFT. On the contrary, the device prepared on a bare SiO_2 showed only p -channel operation and no saturation current for the n -channel configuration at all under the same measurement condition. The corresponding transfer characteristics of the TFT were presented in Fig. 5. We obtained field-effect mobilities of $0.21 \text{ cm}^2/(\text{Vs})$ for hole, and $5.3 \times 10^{-2} \text{ cm}^2/(\text{Vs})$ for electron, respectively. The threshold voltage was calculated to be -12.8 V for p -channel operation and 68.0 V for n -channel. Unfortunately, after this field-effect measurement in a vacuum, the ambipolar transport behavior disappeared on the exposure of the device to air.

3.3 Thickness dependence of the PMMA layer on transistor characteristics

The relationship between the thickness of the PMMA spacer and the carrier transport properties of the pentacene transistor was examined. The parameters obtained from the TFTs with various thickness PMMA layers were summarized in Table 1. In the case of all specimens in Table 1, pentacene films showed similar X-ray diffraction profiles and surface morphologies, suggesting that structures of pentacene films were

quite identical. Nevertheless, as shown in Table 1, both the field-effect mobilities for hole and electron became higher with the smaller thickness of PMMA. For the largest thickness (222 nm) of PMMA, the gate insulator broke down at $V_G > 100$ V before the commencement of n -channel operation.

4. Discussion

4.1 *Influence of the PMMA layer on the hole transport in pentacene TFTs*

The value of the hole mobility measured for pentacene TFTs with the PMMA layer was smaller than those fabricated on bare SiO₂ under the similar evaporation condition (0.76 cm²/(Vs) on average in our specimens). This consequence presumably reflects the grain size of pentacene as shown in Fig. 3. Namely, the larger grain size leads to the larger field-effect mobility. In addition, we previously reported that ultrathin PMMA film was quite effective for covering electron traps on bare SiO₂ [15,16]. From this viewpoint, it might be possible that the PMMA layer reduced acceptor species (hydroxyls) at the pentacene/insulator interface and degraded the hole accumulation and transport in the p -channel region.

4.2 *Influence of the PMMA layer on the electron transport in pentacene TFTs*

In conventional pentacene transistors, the electron injection is strongly interfered with a large energy barrier between a low LUMO level and metal electrodes with high work functions such as Au, platinum, and indium tin oxide (ITO), leading to the suppression of *n*-channel operation of TFTs. Actually, the threshold voltage for *n*-channel operation was much larger than that for *p*-channel operation.

In general, the vacuum level shift at the semiconductor-metal interfaces, caused by the formation of dipole layers, should be considered [22]. Kaji et al. reported that the carrier type was determined by the interface dipole layer by itself in the same aluminumchlorophthalocyanine TFT [23]. However, as previously reported, electron traps derived from hydroxyls on oxide insulators can be reduced by covering the insulator surface with hydroxyl-free polymer dielectrics such as PMMA [9-12,15,16]. At present, we suppose that *n*-channel conduction in this study was mainly caused by the suppression of electron traps with the ultrathin PMMA layer.

Some previous works showed that PVA is also effective as gate spacer for *n*-channel conduction in pentacene TFTs, although PVA is a hydroxyl-group-rich polymer [7,8,13]. It was firstly reported by Singh et al. that the pentacene TFT with the PVA gate dielectric revealed ambipolar transport [8], where hole and electron mobilities are higher than the values obtained in this study. However, the pentacene TFT with the

PVP dielectric, which is also rich in hydroxyl group, was not driven in *n*-channel operation [8]. It can be expected that the electron trapping effect of hydroxyls in PVA and PVP is weaker than silanol (SiOH) on SiO₂. In addition, each molecular unit of PVP owns one benzene ring which might tend to capture electrons at the semiconductor/insulator interface, while PVA has no π -bonding. That can be one of the reasons why the *n*-channel conduction was possible only in the case of PVA. Another possible reason suggested by Takebayashi et al. is that sodium ions in the PVA dielectric can alter the injection barrier at the Au/pentacene and enable the *n*-channel conduction [13].

PMMA (without any hydroxyl group) has carbonyl groups which can possibly become bound to hydroxyls on SiO₂ surface via hydrogen bonding, leading to the decrease of electron traps deriving from SiOH. This comparison with PVA and PVP indicates that PMMA has some advantages as gate dielectric for enhancing the electron accumulation in OTFTs.

The electron mobility of single-component ambipolar pentacene TFTs with Au source-drain electrode obtained here ($5.3 \times 10^{-2} \text{ cm}^2/(\text{Vs})$) is considerably higher than the value ($1.0 \times 10^{-4} \text{ cm}^2/(\text{Vs})$) obtained in another report where PMMA layers thicker than 100 nm were deposited on SiO₂ gate insulators [10]. As for the hole mobility, the

value ($9.0 \times 10^{-2} \text{ cm}^2/(\text{Vs})$) reported in the same previous paper [10] is comparable to that ($0.21 \text{ cm}^2/(\text{Vs})$) obtained in our study. This result suggests that the extent of π -overlap between molecules and distribution of crystalline grains and grain boundaries in pentacene films are not so different in these studies. From this consideration, it can be said that thinner PMMA layer plays the most crucial role for the drastic improvement of electron transport properties in pentacene TFTs.

The carrier transport in OTFTs with many grain boundaries can be explained by hopping conduction between localized states [24], taking into account the field-effect mobility obtained in this work. According to this model, charges accumulated by an applied gate voltage will fill the lower-lying (deep) states of the organic semiconductor. Then, additional charges induced by further gate-biasing can hop between (shallow) neighboring sites with less activation energy. And this mechanism can rationalize the dependence of the field-effect mobility on the applied gate bias at very low drain-source voltages [25,26]. This gate-bias effect may be applicable for explaining the PMMA thickness dependence of the field-effect mobility as shown in Table 1. Accordingly, thinner PMMA layer probably leads to more efficient carrier accumulation at lower gate voltages and gives rise to the increase of the field-effect mobility.

5. Conclusions

In summary, we demonstrated high-mobility, ambipolar pentacene thin-film transistors with the ultrathin PMMA gate buffer layer and Au source-drain electrode. In particular, the excellent value of electron field-effect mobility ($5.3 \times 10^{-2} \text{ cm}^2/(\text{Vs})$) for pentacene thin film was obtained. Ultrathin PMMA layer can work effectively for both eliminating electron traps and promoting electron accumulation. As a result, *n*-channel transport behavior appeared in pentacene TFTs. This technique is very promising for developing high-performance organic inverters like CMOS and investigating “trap-free” carrier transport in organic semiconductors.

Acknowledgements

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(Figure captions)

Fig. 1. (a) Energy band diagrams of a Au electrode and pentacene. (b) Structure of a pentacene TFT with PMMA buffer layer.

Fig. 2. X-ray reflectivity profile for the ultrathin PMMA film prepared onto a SiO₂/Si substrate. The black solid line is the curve best-fitted for the experimental result (open circles).

Fig. 3. AFM images of pentacene thin films prepared on (a) PMMA-coated SiO₂ and (b) a bare SiO₂ film (scanning area: 10 μm \times 10 μm). (c) An X-ray diffraction profiles for pentacene films deposited on PMMA-coated SiO₂.

Fig. 4. Output characteristics of the pentacene TFT with the 8-nm-thick PMMA layer (a) in the *p*-channel and (b) *n*-channel mode. The values of gate voltage (V_G) under each measurement were indicated in these profiles.

Fig. 5. Transfer characteristics of the pentacene TFT with the 8-nm-thick PMMA layer in ambipolar operation. The values of drain voltage (V_D) under each measurement were shown in this profile.

(Table caption)

Table 1 Parameters obtained from the pentacene TFTs with the PMMA spacers and gold source-drain electrodes.

Figure1

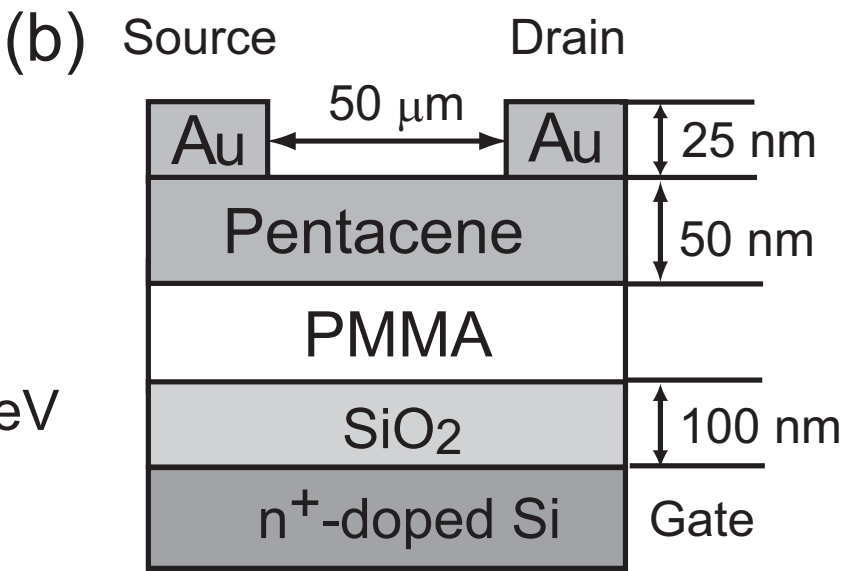
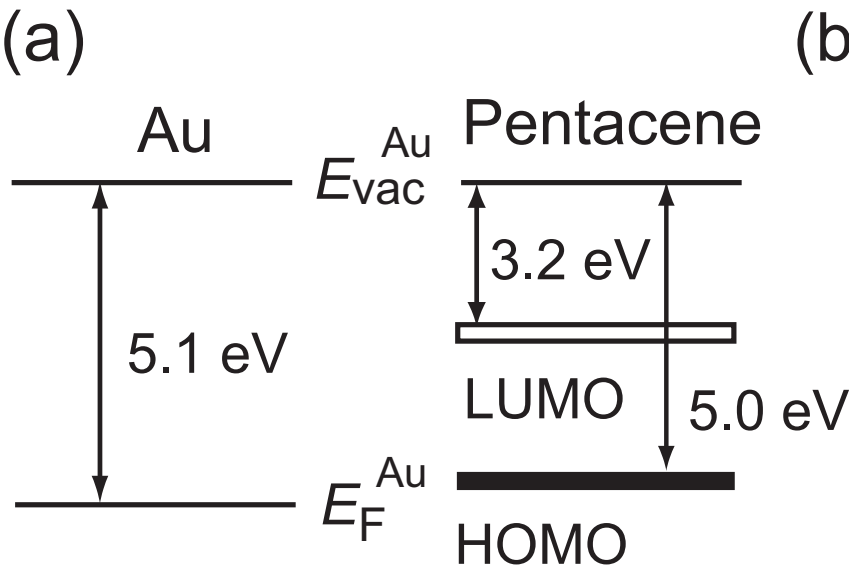


Figure2

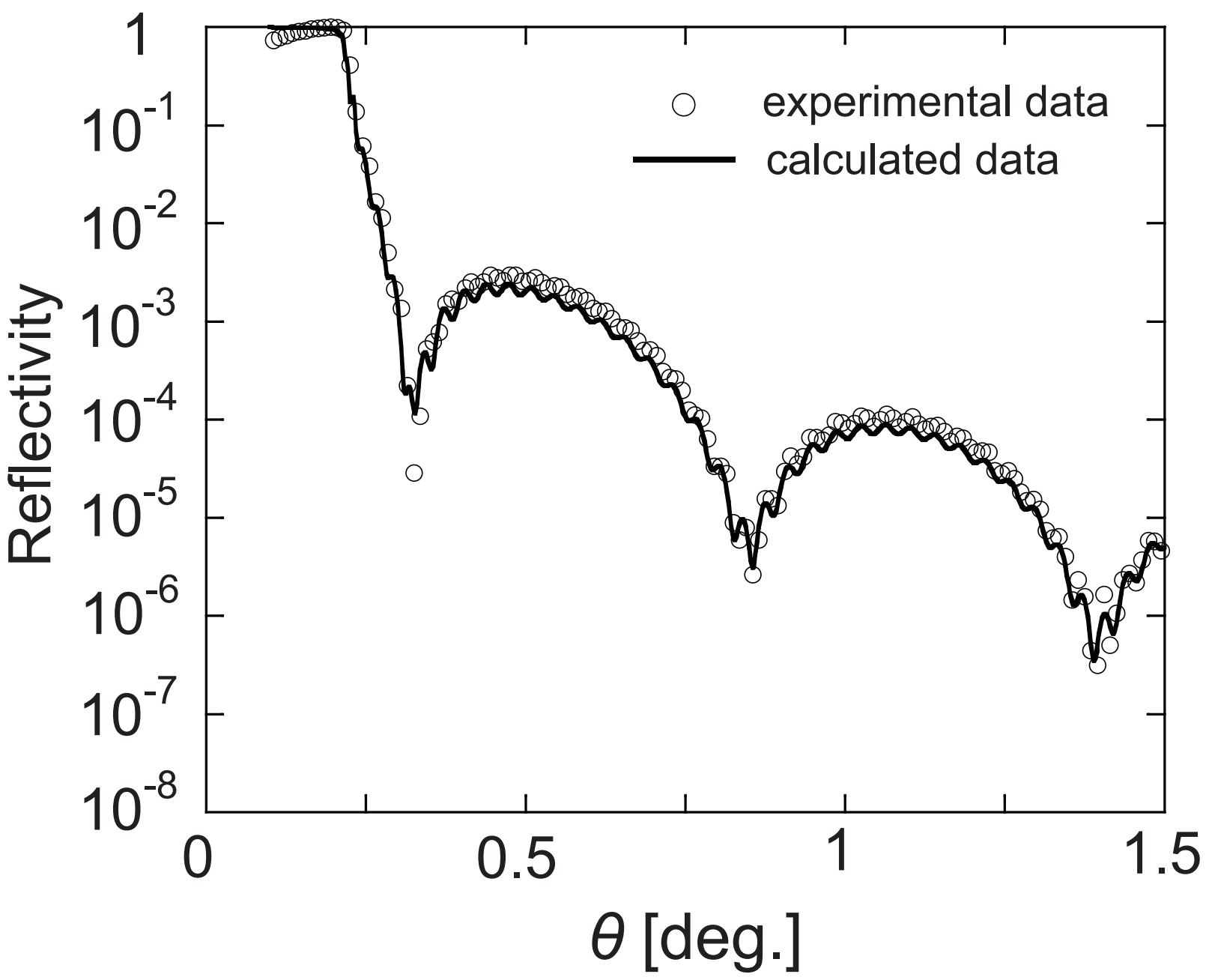


Figure3

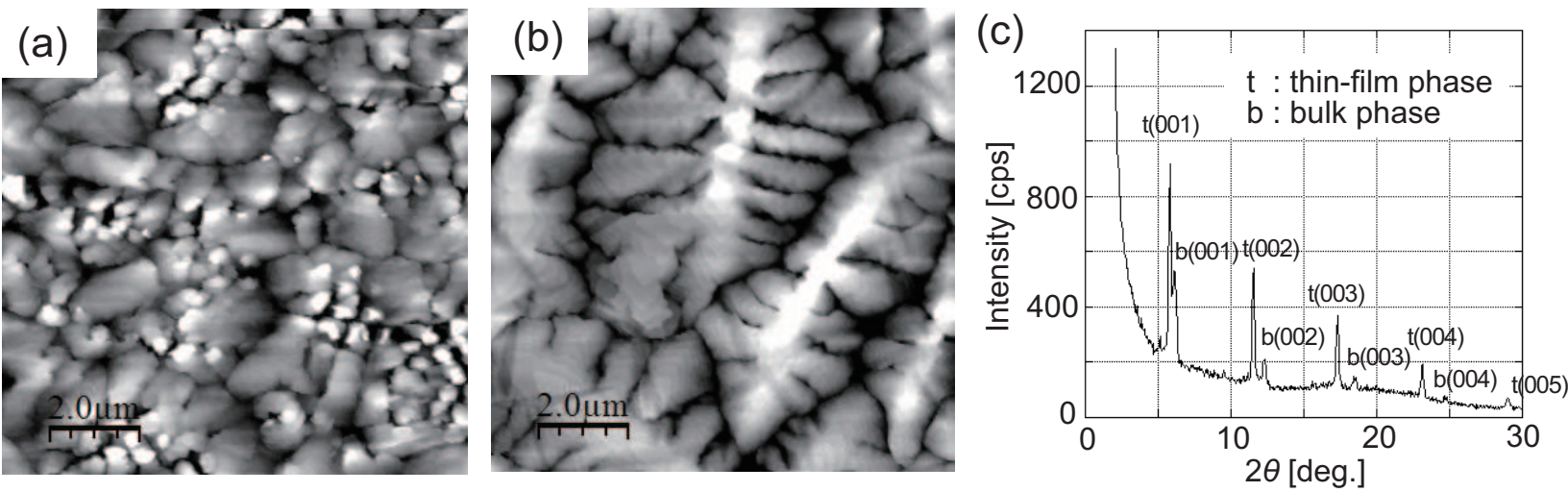


Figure 4

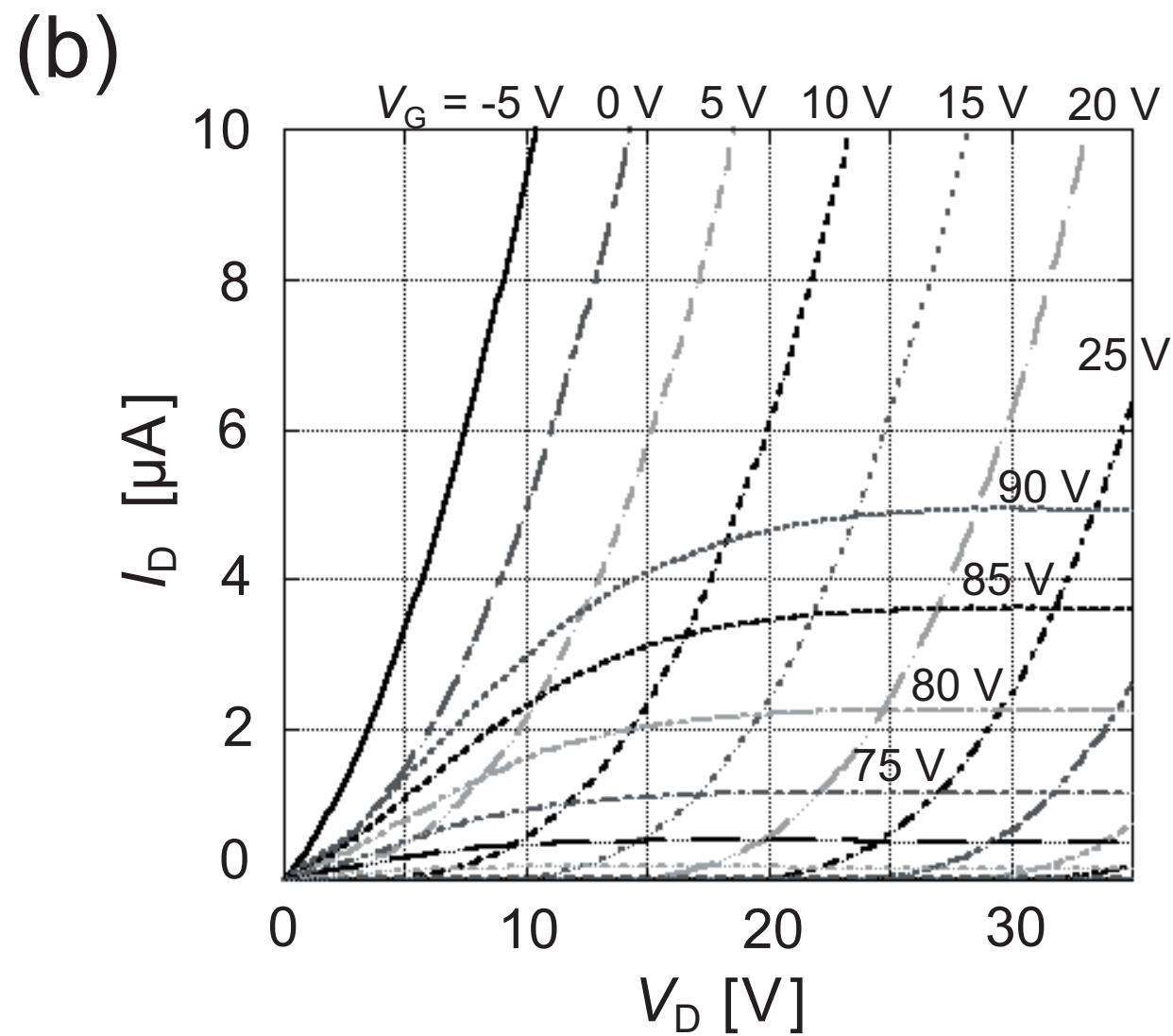
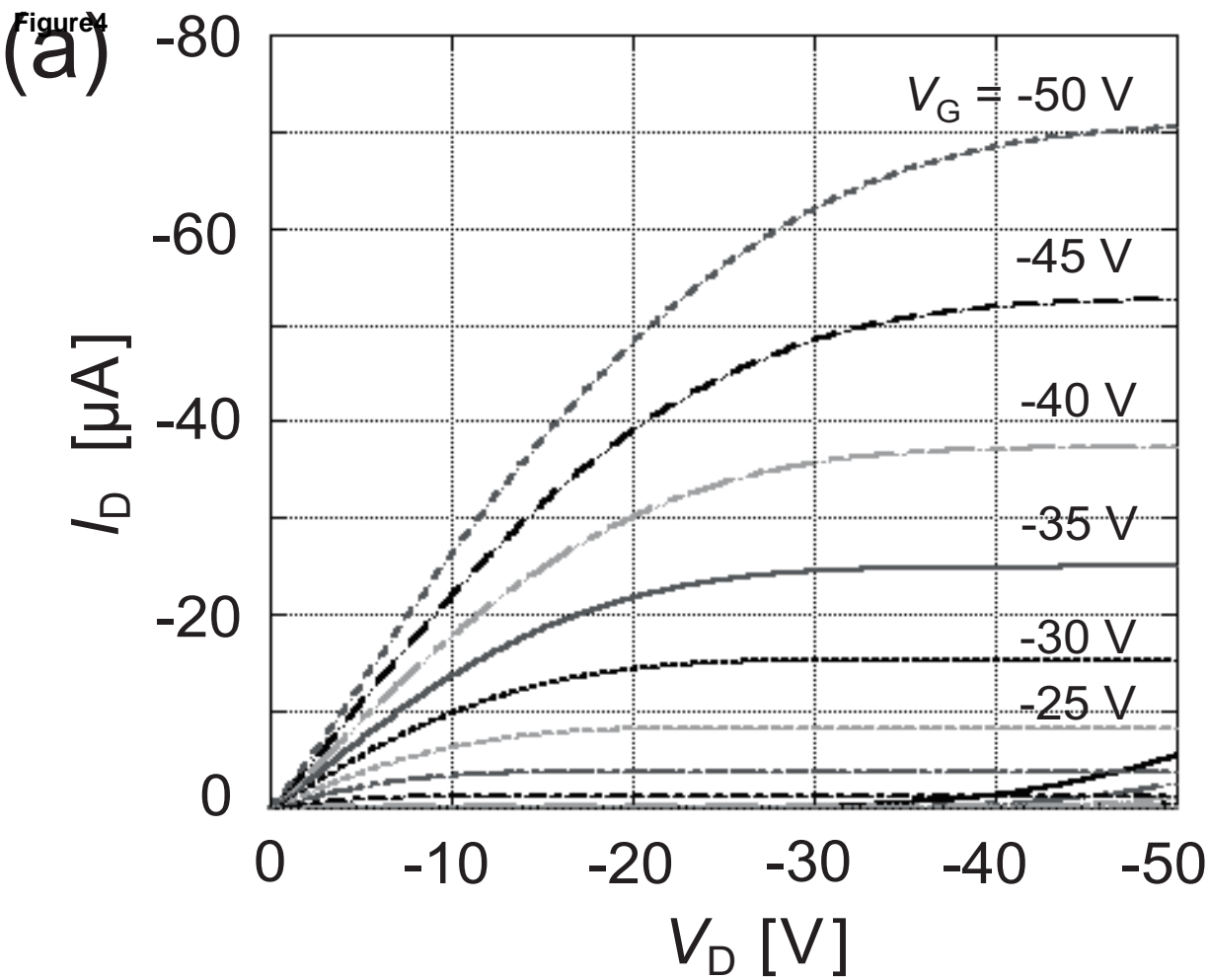


Figure5

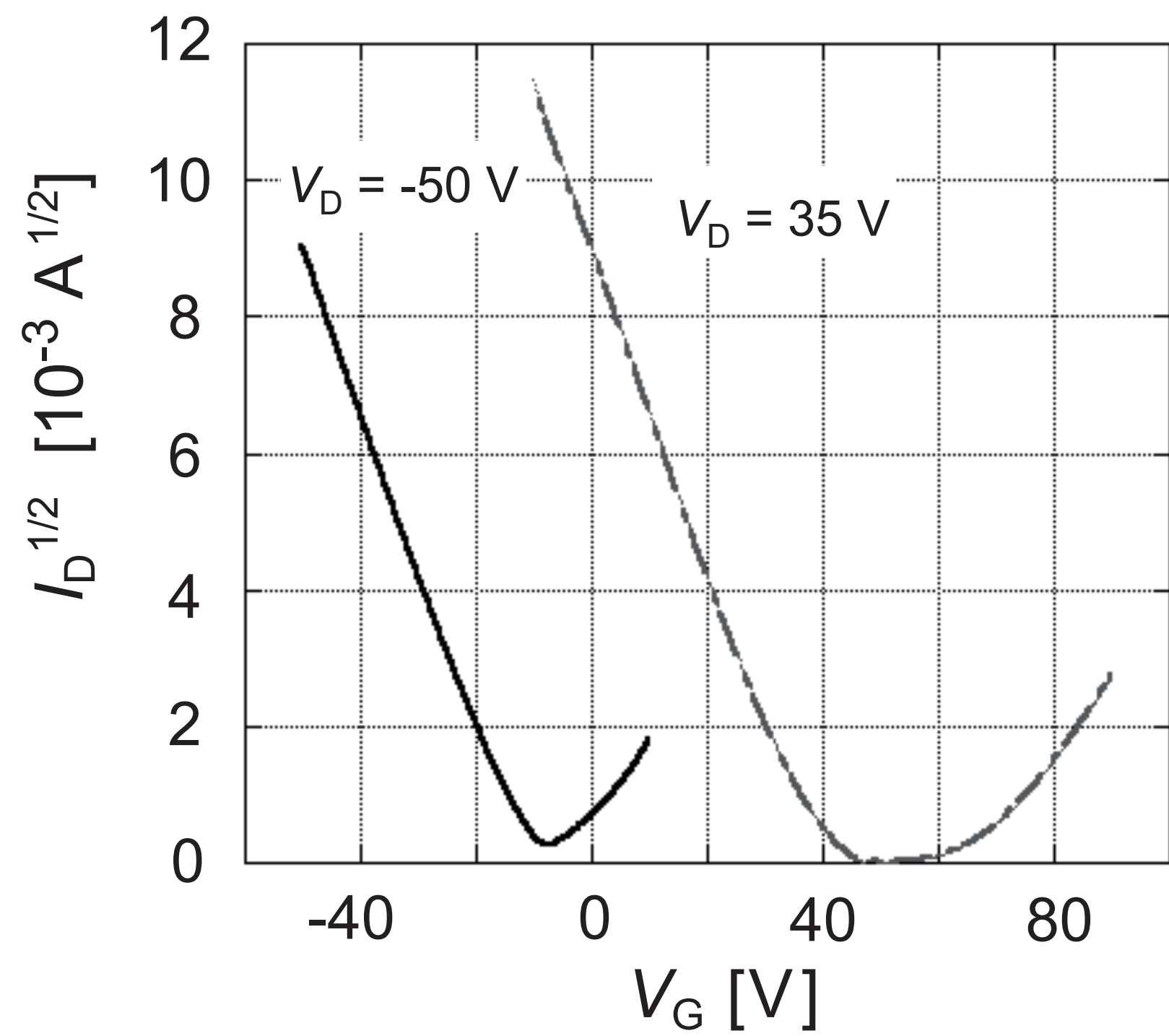


Table1

Thickness of PMMA (nm)	Gate Capacitance C_i (nF/cm ²)	Hole mobility μ_h (cm ² /(Vs))	Electron mobility μ_e (cm ² /(Vs))	V_T for hole (V)	V_T for electron (V)
8.0	29.3	0.21	5.3×10^{-2}	-12.8	68.0
118	15.8	0.16	2.5×10^{-2}	-17.9	61.1
222	9.17	0.14	----- ^a	-28.5	----- ^a

^a *N*-channel conduction was not observed.